AMENDMENT TO THE CLAIMS

Please amend the presently pending claims as follows:

1. (Previously Presented) Device for comparing two words N and P of n bits each, which includes at least one level-1 comparator block which itself includes:

n basic comparator blocks, each enabling the bits Ni and Pi of position i of words N and P to be compared, with i being between 0 and n-1, and each including:

a first sub-block for generating at its output, forming a first output of the basic comparator block, a first signal indicating whether or not the bits Ni and Pi are equal;

a second sub-block enabling a second signal, indicating which of the bits Ni and Pi is greater, to be generated at its output; and

a third sub-block enabling the second signal to pass to a second output of the basic comparator block, if the first signal does not indicate an equality of the bits Ni and Pi, and otherwise enabling the second signal to be blocked;

means for generating a third signal at a first output of the level-1 comparator block, indicating that the numbers N and P are equal if the n first signals indicate that the n bits Ni and the n bits Pi are equal, and otherwise indicating that the numbers N and P are not equal; and

first selective passage means enabling the second output of a basic comparator block to be selectively connected to a second output of the level-1 comparator block, which basic comparator block, from among the basic comparator blocks having a second signal at their second output, processes higher-order bits, with the signal present at the second output of the level-1 comparator block indicating which of the numbers N and P is greater.

2. (Currently Amended) Device according to claim 1, wherein the first sub-block includes an

~~"exclusive-OR"~~ exclusive-OR gate receiving the bits Ni and Pi at the input.

3. (Currently Amended) Device according to claim 1, wherein the second sub-block includes an ~~"OR"~~ OR gate receiving, at an input thereof, the bit Pi and, via an inverter, the bit Ni.

4. (Currently Amended) Device according to claim 1, wherein the third sub-block includes a ~~"selective passage"~~ selective passage gate of which the input is connected to the output of the second sub-block and which is controlled by the output of the first sub-block.

5. (Currently Amended) Device according to claim 1, wherein the means for generating the third signal, at the first output of the level-1 comparator block, include an ~~"OR"~~ OR gate of which the inputs are connected to the first outputs of the basic comparator blocks.

6. (Currently Amended) Device according to claim 1, wherein the first selective passage means include:

means enabling the second output of the basic comparator block processing the high-order bits Nn-1 and Pn-1 to be directly connected to the second output of the level-1 comparator block; and

for each of the other basic comparator blocks processing Nj and Pj bits, with j being between 0 and n-2, means for connecting the second output of the basic comparator block to the second output of the level-1 comparator block, via a ~~"selective passage"~~ selective passage gate ~~(pass-gate)~~ controlled by the output of an ~~"OR"~~ OR gate of which one inputs are connected to the first outputs of the basic comparator blocks of higher order than j.

7. (Previously Presented) Device according to claim 1, wherein said at least one level-1 comparator block also includes means for storing the value present at the second output of the level-1 comparator block.

8. (Currently Amended) Device according to claim 7, wherein the storage means include:

a ~~"NOT OR"~~ NOT OR gate of which a first input is connected to the second output of the level-1 comparator block and a second input is connected, via an inverter, to the first output of the level-1 comparator block; and

a low-current inverter connecting the output of said ~~"NOT OR"~~ NOT OR gate to the first input of said ~~"NOT OR"~~ NOT OR gate.

9. (Previously Presented) Device according to claim 1, wherein the device includes at least one level-2 comparator block which itself includes:

q level-1 comparator blocks, with $q \geq 2$, each including a portion of the n basic comparator blocks;

means for generating a fourth signal at a first output of the level-2 comparator block, indicating that the numbers N and P are equal if the first outputs of the q level-1 comparator blocks indicate that the bits that they compare are equal, and otherwise indicating that the numbers N and P are not equal; and

second selective passage means, enabling the second output of a level-1 comparator block to be selectively connected to a second output of the level-2 comparator block, which level-1 comparator block, from among the level-1 comparator blocks having a second signal at their second output, processes higher-order bits, with the signal present at the second output of the level-2 comparator block indicating which of the numbers N and P is greater.

10. (Currently Amended) Device according to claim 9, wherein the means for generating the fourth signal, at the first output of the level-2 comparator block, include an ~~"OR"~~ OR gate of which the inputs are connected to the first outputs of the level-1 comparator blocks.

11. (Currently Amended) Device according to claim 9, wherein the second selective passage

means include:

means enabling the second output of the level-1 comparator block processing the high-order bits to be connected to the second output of the level-2 comparator block, via a ~~"selective passage"~~ selective passage gate controlled by the first output of the level-1 comparator block processing the high-order bits; and

for each of the other level-1 comparator blocks, means for connecting the second output of the level-1 comparator block to the second output of the level-2 comparator block, via a ~~"selective passage"~~ selective passage gate controlled by the output of an ~~"OR"~~ OR gate of which one input is connected, via an inverter, to the first output of said level-1 comparator block, and of which the other inputs are connected to the first outputs of the higher-order level-1 comparator blocks.

12. (Previously Presented) Device according to claim 9, wherein said at least one level-2 comparator block also includes means for storing the value present at the second output of the level-2 comparator block.

13. (Currently Amended) Device according to claim 12, wherein the storage means include:

a ~~"NOT OR"~~ NOT OR gate of which a first input is connected to the second output of the level-2 comparator block and a second input is connected, via an inverter, to the first output of the level-2 comparator block; and

a low-current inverter connecting the output of said ~~"NOT OR"~~ NOT OR gate to the first input of said ~~"NOT OR"~~ NOT OR gate.

14. (Previously Presented) Device according to claim 1, wherein the device includes at least one level-k comparator block, with $k \geq 2$, which itself includes:

p level-k-1 comparator blocks, with $p \geq 2$;

means for generating a fifth signal at a first output of the level-k comparator block, indicating that the numbers N and P are equal if the first outputs of p level-k-1

comparator blocks indicate that the bits that they are comparing are equal, and otherwise indicating that the numbers N and P are not equal; and

third selective passage means, enabling the second output of a level-k-1 comparator block to be selectively connected to a second output of the level-k comparator block, which level-k-1 comparator block, from among the level-k-1 comparator blocks having a signal at their second output, processes higher-order bits, with the signal present at the second output of the level-k comparator block indicating which of the numbers N and P is greater.

15. (Previously Presented) Device according to claim 1, wherein each selective passage means an N-Type transistor mounted parallel with respect to a P-Type transistor.

16. (Previously Presented) Device according to claim 1, wherein the device is produced in the form of a wired circuit.

17. (Previously Presented) Device for comparing two words N and P of n bits each, which includes at least one level-1 comparator block which itself includes:

n basic comparator blocks, each enabling the bits Ni and Pi of position i of words N and P to be compared, with i being between 0 and n-1, and each including:

a first sub-block for generating at its output, forming a first output of the basic comparator block, a first signal indicating whether or not the bits Ni and Pi are equal;

a second sub-block enabling a second signal, indicating which of the bits Ni and Pi is greater, to be generated at its output; and

a third sub-block enabling the second signal to pass to a second output of the basic comparator block, if the first signal does not indicate an equality of the bits Ni and Pi, and otherwise enabling the second signal to be blocked;

a circuit which generates a third signal at a first output of the level-1 comparator block,

indicating that the numbers N and P are equal if the n first signals indicate that the n bits Ni and the n bits Pi are equal, and otherwise indicating that the numbers N and P are not equal; and

a first selective passage gate enabling the second output of a basic comparator block to be selectively connected to a second output of the level-1 comparator block, which basic comparator block, from among the basic comparator blocks having a second signal at their second output, processes higher-order bits, with the signal present at the second output of the level-1 comparator block indicating which of the numbers N and P is greater.

18. (Previously Presented) A method of comparing two words N and P of n bits each, the method comprising:

comparing the bits Ni and Pi of position i of words N and P, with i being between 0 and n-1, which comprises for each bit i:

generating at a first output a first signal indicating whether or not the bits Ni and Pi are equal;

generating a second signal indicating which of the bits Ni and Pi is greater; and

passing the second signal to a second output if the first signal does not indicate an equality of the bits Ni and Pi, and otherwise blocking the second signal from being passed to the second output;

generating a third signal at a first comparator output indicating that the numbers N and P are equal if the n first signals indicate that the n bits Ni and the n bits Pi are equal, and otherwise indicating that the numbers N and P are not equal; and

selectively passing the second signals that are passed to respective second outputs to a second comparator output so as to indicate which of the numbers N and P is greater.